IN THE CLAIMS

Please amend claims 1-10 and 15-18. All claims have been provided as a courtesy to the Examiner.

---

1. (Amended) A system comprising:

a system memory controller; and

a first memory module comprising:

a first plurality of memory devices;

a first memory module controller coupled to the system memory controller and the first plurality of memory devices[; and], the first memory module controller being configured to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format for the first plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

[a first plurality of memory devices coupled to the first memory module controller.]

2. (Amended) The system of claim 1, further comprising:

a first memory bus coupled between the system memory controller [first memory module] and the first memory module controller.

3. (Amended) The system of claim 2, wherein the first memory bus comprises a signal line for a clock signal.

4. (Amended) The system of claim 2, wherein the first memory bus comprises:

a signal line for a handshake signal that indicates when the first memory module controller is communicating data to the system memory controller.

5. (Amended) The system of claim 2, further comprising:

a second memory bus coupled between the first memory module controller and the first plurality of memory devices.

6. (Amended) The system of claim 5, wherein the second memory bus comprises:

a signal line for a clock signal.

7. (Amended) The system of claim 5, wherein the first memory bus operates at a first data rate and the second memory bus operates at a second data rate, and wherein the first data rate is different than the second data rate.

8. (Amended) The system of claim 5, wherein the first memory bus has a first number of signal lines and the second memory bus has a second number of signal lines, and wherein the first number of signal lines is different than the second number of signal lines.

9. (Amended) The system of claim 5, wherein the first memory module controller comprises:

request handling circuitry [structured] configured to receive [a] the first memory transaction from the first memory bus; and

control logic coupled to the request handling circuitry and configured to reformat the first memory transaction into [generating a] the second memory transaction on the second memory bus [corresponding to the first memory transaction on the first bus].

10. (Amended) The system of claim 2, wherein the first memory bus is configured to carry [carries] time-multiplexed data and address information, and wherein the second memory bus includes separate address and data lines.

11. (Unchanged) The system of claim 1, wherein the first memory module is a dual in-line first memory module (DIMM).

12. (Unchanged) The system of claim 1, wherein the first memory module is a single in-line first memory module (SIMM).

13. (Unchanged) The system of claim 1, wherein the first plurality of memory devices comprise volatile memory devices.

14. (Unchanged) The system of claim 1, wherein the first plurality of memory devices comprise nonvolatile memory devices.

15. (Amended) The system of claim 1, further comprising a second memory module [comprising] including:

a second plurality of memory devices;

a second memory module controller coupled to the system memory controller and the second plurality of memory devices [; and] , the second memory module controller being configured to receive from the system memory controller a third memory transaction in the first format and to convert the third memory transaction into a fourth memory transaction in the second format for the second plurality of memory devices, the second format of the fourth memory transaction being different from the first format of the third memory transaction.

[a second plurality of memory devices coupled to the second memory module controller.]

16. (Amended) The system of claim 15, wherein the first plurality of memory devices store [stores] data in a different way than the second plurality of memory devices.

17. (Amended) A system comprising:

a system memory controller;

a memory bus coupled to the system memory controller; and

a memory unit [comprising] including:

a plurality of memory devices;

a memory module controller coupled to the memory bus and the plurality of memory devices[; and], the memory module controller being configured to receive a first memory transaction from the memory bus in a first format and to convert the first memory transaction into a second memory transaction in a second format to at least one of the plurality of memory devices, the second format of the second memory transaction being different from the first format of the first memory transaction.

[a plurality of memory devices coupled to the memory module controller, wherein the memory module controller receives a first memory transaction from the memory bus in a first format and provides a second memory transaction in a second format to at least one of the second plurality of memory devices.]

18. (Amended) A method of communicating a memory transaction between a system memory controller and at least one of a plurality of memory devices on a